deep-submicron HEMTs and RTDs may enable future high-speed digital integrated circuits with data rates approaching 100 GHz.

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REFERENCES


Abstract—A simple post-processing technique allowing Cu inductors to be added to integrated circuits fabricated in technologies providing only Al metallization is presented. The inductors use a 4-μm thick electroless plated Cu layer to minimize resistance, and are formed over a 9-μm thick polyimide dielectric to reduce substrate losses. Inductors optimized for 2.5-GHz had $Q$ as high as 17. The effectiveness of the post-processing technique is demonstrated by application to a voltage-controlled oscillator (VCO) fabricated in a commercial bipolar technology with Al metallization. Circuits with post-processed Cu inductors gave a phase noise of $-106$ dBc/Hz at 100 kHz offset from a 2-GHz carrier, while control circuits with Al inductors gave a phase noise of only $-101$ dBc/Hz at 100 kHz offset from a 1.8-GHz carrier and had higher power consumption.

Index Terms—Bipolar transistor circuits, copper interconnect, induc- tors, phase noise, polyimide films, voltage-controlled oscillator (VCO).

I. INTRODUCTION

When inductors are made in Si technology with Al metallization the relatively high interconnect resistance and substrate losses typically limit $Q$ to values less than 10. This restricts the performance of many fully-integrated RF circuit blocks, such as voltage-controlled oscillators (VCOs). To improve the performance of an integrated inductor, it is necessary to isolate the device from the substrate and use a low-resistance metallization. Substrate isolation can be provided by placing thick layers of low-k dielectric beneath the inductors [1], and the use of Cu metallization in place of Al can provide a 40% improvement in line resistance [1], but to date only a limited number of manufacturers offer Cu metallization.

This brief presents a simple post-processing technique to add high-$Q$ Cu inductors to integrated circuits fabricated using technologies which otherwise only provide Al metallization. The inductors are formed over a 9-μm thick layer of polyimide dielectric to reduce substrate losses and give a high self-resonant frequency. An electroless Cu plating technique provides metal lines up to 4-μm thick with a resistivity of 1.8-μm$\Omega \cdot \text{cm}$, close to that of bulk Cu and only 60% that of sputtered Al.

To demonstrate the effectiveness of the post-processing technique, Cu inductors were added to a VCO fabricated in a commercial 25-GHz fT bipolar technology. The VCO was selected as a demonstration vehicle due to its extreme sensitivity to inductor $Q$. Performance of circuits with post-processed Cu inductors is compared to that of control circuits with Al inductors.

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J. W. M. Rogers was with the Department of Electronics, Carleton University, Ottawa, ON, K1S 5B6 Canada. He is now with the SiGe Microsystems, Ottawa, ON, K2B 8J9 Canada.

V. Levenets was with the Department of Electronics, Carleton University, Ottawa, ON, K1S 5B6 Canada. He is now with ST Microelectronics, Ottawa, ON, K2H 8V4 Canada.

C. A. Pawlowicz was with the Department of Electronics, Carleton University, Ottawa, ON, K1S 5B6 Canada. He is now with Nortel Networks, Ottawa, ON, K1Y 4H7 Canada.

N. G. Tarr, T. J. Smy, and C. Plett are with the Department of Electronics, Carleton University, Ottawa, ON, K1S 5B6 Canada.

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The VCO circuit implemented here is shown in Fig. 1. It is a differential implementation of a Colpitts common-base topology [2]. Capacitors $C_1$ and $C_2$ in parallel with collector-base junction varactors form a negative resistance feedback loop to cause oscillation. Output buffers were added to the circuit to minimize loading by measurement equipment.

One of the most crucial design parameters for a VCO is its phase noise [3]. Leeson’s formula [4] shows that the high-frequency phase noise is inversely proportional to $Q^2$, indicating the importance of $Q$-factor optimization for this circuit. The two major factors determining $Q$ are the dynamic emitter resistance ($r_e$) of transistors $Q_1$ and $Q_2$ and the equivalent parallel resistance of the on-chip inductors. Emitter degeneration ($r_e$) is used to reduce the first loss, and Cu inductors are used to reduce the second loss. Higher $Q$ tanks also boost VCO performance by providing higher output power.

Low-frequency modulated noise can also degrade the phase noise of the oscillator. Currents through the varactor terminals and resistance attached to the terminals must therefore be kept small to minimize noise contributions. However, the currents must also be large enough to provide good VCO output power. Thus the circuit currents and capacitor ratios must be set carefully to attempt to balance these two effects.

Simple square-geometry three turn spiral inductors with $L = 2.6 \text{ nH}$ were designed using ASITIC simulation [5]. ASITIC indicated that best performance would be obtained with the smallest line spacing (5 $\mu \text{m}$) permitted by the lithography and plating technique used. The line width was chosen to be 20 $\mu \text{m}$. Wider metal lines result in lower series resistance, but increase the area required to form a given inductance. This in turn increases substrate losses. The entire VCO occupies a die area of 0.7 $\text{mm} \times 1.1 \text{ mm}$ and the inductors approximately one-third of this area. A photomicrograph of the complete VCO is shown in Fig. 2, with detail of the Cu lines shown in Fig. 4.

### III. Circuit Fabrication

Circuit cores were fabricated in NT25, a 25-GHz $f_T$ bipolar technology with 0.5-$\mu \text{m}$ minimum feature size provided by Nortel Networks of Ottawa, Canada. This technology provides three levels of metallization, with a Metal 3 Al thickness of 2 $\mu \text{m}$. Completed wafers have a dielectric stack approximately 3 $\mu \text{m}$ thick in the field region. The stack consists of thermal oxide, BPSG and SOG. 50 $\mu \text{m}$ square Metal 3 bond pads are left open to allow connection of post-processed inductors to the underlying core circuitry.

Post processing was carried out at the Department of Electronics, Carleton University. To increase the separation of the inductors from the substrate, a thick PI2611 polyimide layer was spun on the wafers and initially baked at 50 $^\circ \text{C}$ for 15 min, 100 $^\circ \text{C}$ for 30 min, and then 150 $^\circ \text{C}$ for 30 min. Following baking, windows to the Metal 3 bond pads were opened through the polyimide by wet etching in tetramethylammonium hydroxide (TMAH) solution at room temperature. The wet etching technique gives a tapered sidewall, which is vital to provide good metal step coverage. After wet etching, the polyimide was fully cured in forming gas. Following manufacturer’s recommendations, the temperature was ramped to 350 $^\circ \text{C}$ at a rate of 4 $^\circ \text{C}$/min and then held at 350 $^\circ \text{C}$ for 30 min. Since the last step in the NT25 flow is a forming gas anneal at 450 $^\circ \text{C}$ the post processing procedure should have minimal impact on device characteristics, although this was not experimentally verified. The cured polyimide had a thickness of 9 $\mu \text{m}$. Based on manufacturer’s data, a dielectric constant of 3.2 is expected.

Electroless Cu plating was then used to form inductors on top of the polyimide layer. Plating avoids the difficulty of etching thick Cu films. A seed (catalytic) layer is required to initiate plating. A stack for seed layer lift-off was formed by applying a 1.4-$\mu \text{m}$ thick layer of photoresist, followed by a 200-nm layer of e-beam evaporated Ti. Using a photoresist mask, windows were etched through the Ti wherever plated Cu traces were to be formed. The Ti was then used as a mask for flood exposure of the underlying resist. After development, this procedure leaves a Ti “lip” overhanging the bottom photoresist layer, facilitating lift-off of the seed. This process is illustrated in Fig. 3.

The seed layer itself consisted of 30 nm Ti, 30 nm Cu, and 30 nm Al deposited by sputtering. The Ti serves as an adhesion layer, while the Al overcoat protects the Cu seed from oxidation. Immediately prior to
seed layer deposition, approximately 100 nm of material was removed from the Metal 3 bond pads by sputter etching. This cleaning procedure was found essential to hold contact resistance between the Al pad and the overlying Cu to an acceptable value.

The Cu plating procedure was based on that described in [6]. The plating solution consisted of cupric sulfate (the source of Cu ions), ethylenediaminetetraacetic acid (complexing agent), formaldehyde (reducing agent), TMAH (pH adjuster), surfactant RE 610 and stabilizer Triton. This plating solution has been chosen because it is suitable for IC manufacturing (alkali-free). The temperature and pH controlled plating bath was maintained at 75 °C and a pH of 11.3, giving a deposition rate of 0.6 μm/h. The solution was placed in a glass beaker capped with a water cooled reflux condenser. A magnetic stir rod was used to agitate the solution. Plating guides were not used. For a spacing of 10 μm between the seed lines, it was found possible to plate up to 4 μm of Cu. Making the lines much thicker would have had minimal impact on the performance of the inductors because the skin depth of Cu at 2 GHz is only about 1.5 μm.

The simplicity of the process used to form the inductors should be stressed. Only two additional masks, one sputtering step, one lift-off step, one etch step, and one plating step are required.

### Table I

<table>
<thead>
<tr>
<th>Metal</th>
<th>Inductance</th>
<th>Q</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al (2μm)</td>
<td>3nH</td>
<td>5.5</td>
<td>2.5GHz</td>
</tr>
<tr>
<td>Cu (0.7μm)</td>
<td>2.6nH</td>
<td>6</td>
<td>2.5GHz</td>
</tr>
<tr>
<td>Cu (1.5μm)</td>
<td>2.6nH</td>
<td>10</td>
<td>2.5GHz</td>
</tr>
<tr>
<td>Cu (2.5μm)</td>
<td>2.6nH</td>
<td>14</td>
<td>2.5GHz</td>
</tr>
<tr>
<td>*Cu (3.5μm)</td>
<td>2.6nH</td>
<td>17</td>
<td>2.5GHz</td>
</tr>
</tbody>
</table>

The performance of completed VCOs was measured using an HP8564E spectrum analyzer. It was found that the frequency could be varied by 120 MHz or about 6%. The VCO core drew approximately 5.5 mA from a 3.3 V supply and provides an output power of −5 dBm per side. A phase noise of better than −106 dBc/Hz (noise power in dB relative to the carrier power in a one Hz bandwidth) at 100 kHz offset was measured. This phase noise is within 1 dB of meeting the GSM requirement of −107 dBc/Hz at 100 kHz offset [7].

The VCO performance was compared to two previously fabricated versions that used an identical topology and Al inductors [2], [8]. The results are shown in Table II. All VCOs were optimized to have almost identical output power to ease comparison. VCO 1 drew 10 mA of current through its core and had a phase noise of −101 dBc/Hz at 100 kHz offset. VCO 2 (a redesign of VCO 1) was re-optimized to have a lower capacitor ratio and therefore used less current than the first design. This also improved the phase noise by 2 dB to give the best performance for the Al VCOs of −103 dBc/Hz at 100 kHz offset. VCO 3 (Cu inductors) had the same capacitor ratio as VCO 1, but used half as much current and still maintained the same output power. It demonstrates the best phase noise performance of −106 dBc/Hz at 100 kHz offset. It is expected that optimization of the capacitor ratio and currents for VCO 3 would result in a similar improvement as was found for VCO 1 and
VCO 2. With this additional refinement, the design should be capable of meeting the GSM requirement for phase noise.

V. CONCLUSIONS

A simple post-processing technique has been presented by which high-\(Q\) Cu inductors can be added to integrated circuit cores formed in technologies which otherwise provide only Al metallization. Cu lines up to 4 \(\mu\)m thick with line spacings down to 5 \(\mu\)m were formed by an electroless plating technique. A Cu resistivity of 1.8 \(\mu\)\(\Omega\)-cm was obtained, close to the bulk value. The Cu inductors were formed over a 9-\(\mu\)m thick polyimide layer to minimize substrate losses. Inductors optimized for operation near 2 GHz gave \(Q\) values as high as 17.

The effectiveness of the post-processing technique was demonstrated by application to a Colpitts VCO circuit fabricated using a commercial bipolar technology. VCO circuits have proven amongst the most difficult RF blocks to integrate, since they are very sensitive to inductor \(Q\)-factors. A VCO using Cu inductors gave a phase noise of \(-106\) dBc/Hz at 100 kHz offset from a 2-GHz carrier. In comparison, the best phase noise obtained from a control VCO, optimized to make use of the 2-\(\mu\)m thick Al inductors normally available in this technology, was \(-103\) dBc/Hz at 100 kHz offset from a 1.9-GHz carrier.

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