CMOS LOW-POWER MICROWAVE FREQUENCY PRESCALERS FOR WIRELESS APPLICATIONS

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Abstract: Future consumer market communication systems are expected to operate at higher frequencies due to congestion within old frequency band allocations. Also advances in CMOS technology make it possible that RF circuits be implemented in this low-power and inexpensive technology.

In this paper we present dual-modulus prescalers in 1.2μm CMOS and 0.8μm BiCMOS operating up to 1.4 GHz and 1.26 GHz respectively.

I. INTRODUCTION

More and more people are turning towards mobile communication in modern society. This field includes not only pagers and mobile telephones but also other systems which can be linked to the mobile communication units e.g. laptop computers are being used to send/receive faxes from remote areas as well as to transfer scientific data. The constraints on such products are that they should be mobile i.e. battery operated, have a long life which means low power, be mechanically robust and most important of all, be inexpensive yet quality products. Contemporary researchers have to keep in mind all these issues for future technology developments.

Due to a huge mobile communication market, most of the frequency bands are already congested which sets very hard constraints for designers. Therefore, it necessary is to go further into higher frequencies and for which, bipolar and GaAs are still the most suitable technologies for RF applications. CMOS is the most commonly used technology in baseband signal processing, it consumes very little power and is the cheapest as well. However, due to recent trends towards submicron device sizes, CMOS is fast becoming the technology for RF circuits so that in the future it might be possible to have RF and DSP circuits on the same CMOS chip [1].

The most important requirement for a mobile communication system such as a cellular phone, is a high resolution frequency synthesizer. Due to stability, drift and phase noise problems, oscillators cannot be used simply for frequency synthesis but one has to employ PLLs. For high resolution, fractional division synthesis is a popular technique because of its simplicity, flexibility and ease in monolithic fabrication as compared to other techniques such as multiloop frequency synthesis. A fractional-N division PLL system is shown in Figure 1, where it can be seen that both the VCO

![Fraction Division Frequency Synthesis](image)

and the prescaler are operating at the highest frequencies, putting additional power dissipation constraints on their design. Whereas the VCO must have a wide tuning range, linear control, low phase-noise and low-power dissipation, the main constraints on the prescaler are that it must operate at the same high frequency as the VCO and consume as little power as possible. In this paper we concentrate on low-power prescaler architectures and circuits.

II. DUAL-MODULUS PRESCALERS

A high resolution frequency synthesizer can be built by replacing the divide-by-N counter with a dual-modulus prescaler/divider in a simple phase-locked-loop. In Figure 1, the prescaler can divide the VCO signal either by N when its control bit MC is low, or by N+1 when MC assumes the logic value of 1. Since the counter is a digital circuit which counts N periods of the clock by sensing specific edges of the incoming waveform, it cannot divide by a fractional number. However, if MC control is fed by a bit stream with alternating 1's and 0's synchronized with its output, i.e. 101010..., then the counter would count N periods of its input for one cycle of its output and N+1 periods for the next output cycle. The VCO can then be locked to an average frequency multiple of N+1/2. This can be expressed mathematically as follows: if the division ratio is chosen to be N for p cycles of the prescaler output and equal to N+1 for q cycles of the same, then once every p + q cycles, the VCO output frequency would be divided on average by a factor.
\[
p\cdot N + q \cdot (N+1) \quad \frac{p\cdot N + q\cdot (N+1)}{p+q} = N + \frac{q}{p+q} \quad (1)
\]

Therefore by selecting an appropriate bit stream pattern frequencies can be synthesized with high resolution.

Dual-modulus prescalers are generally counters, which are classified as sequential circuits. The simplest form of sequential circuits are D-type flip-flops. The D-type flip-flops themselves are constructed by cascading two level sensitive latches. For high speed applications, static circuits used as latches/flip-flops prove to be too slow, dynamic circuits are thus employed. The structure of a dual-modulus prescaler is shown in Figure 2. The first stage is a synchronous (Johnson’s) counter and is built to divide by P or P+1 (P/P+1); usually these numbers are 2/3, 3/4, 4/5 or 8/9 etc.

The second stage is usually a fixed division ratio asynchronous (ripple) counter and output bits from the ripple counter are decoded to provide the first stage modulus depending on the bit value at the modulus control input MD. Since the first stage operates at highest frequencies, its design is most critical, the second stage operates only at a lower frequency of \( f_{IN}/P \) (max.). In the next section we present two prescalers which can achieve operation above 1000 MHz.

**II. PRESCALERS WITH DIFFERENTIAL-LOGIC LEVEL-TRIGGERED LATCHES**

A frequency divider circuit based on differential logic latches was proposed in [2], [3]. The main idea of the design was that in order to achieve high speed with conventional CMOS technology, circuit design must also be improved to take maximum advantage of devices of the order of 1\( \mu \)m or smaller gate length. This was achieved by reducing the circuit complexity. In Figure 3(a) a sequential circuit is shown which is composed of edge triggered D-type flip-flops and clocked by the same signal. Some combinatorial logic circuits are also present. Generally the edge triggered flip-flops are composed of master-slave latches. In this design the maximum operating frequency of the circuit was increased by removing one latch from the flip flop resulting in a sequential circuit as shown in Figure 3(b). This would reduce the total delay through the flip flop, \( T_m \) or \( T_s \), but since latches are level triggered, the clock duration during which latches are transparent must be kept to a certain minimum. Although this narrows down the operating frequency range, it is not critical since PCS applications usually work in a narrow band allocation.

The first stage of the circuit uses single phase clock and differential-logic level-triggered latches connected as a two bit Johnson’s counter. The circuit is shown in Figure 4 [2], [3]. The circuit uses positive feedback by a cross coupled pair of p-type MOSFETs. When the clock signal is high, the inverting buffers drive the D and \( \bar{D} \) inputs of the next latch to toggle the cross coupled transistors. The second stage of the circuit is a ripple counter made with two TSPC flip-flops to make a divide-by-15/16 prescaler. This design was fabricated in two technologies. First implementation was done in 3\( \mu \)m CMOS3 DLM technology [2]. It achieved a maximum frequency of approximately 330 MHz while consuming 12mW at 5 Volts supply.
The second implementation was done in 1.2µm CMOS4S technology [2], [3]. Specific characteristics are given in Table 1. For further information please refer to [2], [3].

<table>
<thead>
<tr>
<th>Freq</th>
<th>Power</th>
<th>( V_{in} ) (rms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 GHz</td>
<td>10 mW</td>
<td>260 mV, ( V_b = 2.29 ) V</td>
</tr>
<tr>
<td>1.4 GHz</td>
<td>12.6 mW</td>
<td>210 mV, ( V_b = 2.12 ) V</td>
</tr>
</tbody>
</table>

\( V_b = \) Bias voltage at input

### III. PRESCALERS WITH DYNAMIC CIRCUITS

Several types of dynamic flip-flops have been proposed in [3], [4], [5], [6], [7]. These circuits have a lower limit of operating frequency set by the dynamic circuit nature and a high frequency limit set by the delays. In [4] and [5] improved flip-flop circuits were presented making them pseudo-static, thus increasing the low frequency limit of operation. In this section we present a prescaler designed with dynamic D-type flip-flops.

The dual-modulus prescaler has been implemented in 0.8µm BiCMOS technology with division ratios of 31/32. The measured operating frequency is 1260 MHz while consuming 12 mW at 5 volts. As discussed earlier, this has two stages, first stage being a Johnson's counter and the second a three stage ripple counter.

#### First Stage Design

The first stage block diagram is shown in Figure 5 with the control logic. This stage is a 3/4 divider. When the MC input is high, it keeps the node X below the threshold voltage so that the transistor M1 stays off. In this mode the circuit performs its regular division by 4. When MC is low, then signals coming from \( Q'_1 \) and \( Q'_2 \) are sensed and when both of them are low M1 pulls down D2. This causes the counter to jump from state \( Q_2Q_1=11 \) to 00 instead of going to \( Q_2Q_1=10 \). The effect is that it skips one cycle and thus it counts three periods rather than four. This logic, as seen here, is implemented with NMOS transistors and it senses the signals while the state changes occur. This way the delay which is present due to series logic is much reduced, however only at the expense of some extra current during one cycle.

The transistor level circuit used for the D-type flip-flops is shown in Figure 6. It uses a true single phase clock to form a positive edge triggered D-type flip flop. The circuit was simulated in HSPICE and has a (simulated) working range from 610 MHz to 1100 MHz.

#### Second Stage Design

The second stage also utilizes dynamic flip-flops. Once the frequency is divided down by a factor of 3 or 4, the input frequency range for the second stage is in the range of 150

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\[ \text{Figure 5: Improved Dynamic Flip-Flop} \]

MHz to 400 MHz which means that the flip-flops need to be slower. The flip-flops from the first stage cannot be used here since below 600 MHz, the precharged nodes tend to lose their charges due to leakage currents resulting in spurious behavior.

To improve the circuit behavior at low frequencies a modified circuit is shown in Figure 7 [4], [5]. A feedback transistor keeps the node \( Q'_1 \) high while another transistor is added to avoid glitches normally occurring in this circuit. The glitch can come when node A is high and the added
transistor, driven by an inverter from node A, removes the hazard [4], [6]. With these improvements this circuit would function properly well below 10 MHz with proper design.

**Measurement Results**

In Figures 8, 9 and 10, some performance curves are shown for the 0.8μm BiCMOS prescaler. The power-frequency dependence is shown in Figure 8. The power dissipation at 1250 MHz is only 12 mW. The power dissipation at 900 MHz is 11 mW (divide by 31). The linear relationships can be observed up until 1075 MHz after which the curves flatten. The flattening can be attributed to decreasing amplitudes of the internal nodes. Figure 9 shows the input signal sensitivity curves indicating a quite wide region of operation. Finally, Figure 10 shows the maximum frequency as a function of power supply variation from 3 volts to 5 volts.

**IV. CONCLUSIONS**

We presented two low-power dual-modulus prescaler circuits implemented in CMOS. First we presented a circuit which uses differential-logic level-triggered latches and dissipates only 12.5 mW @ 5V supply while operating at 1.4 GHz. The second circuit uses dynamic flip-flops, works up to 1.26 GHz while dissipating only 12 mW @ 5V supply.

It can be said that CMOS technology can be regarded as an RF technology for applications operating below 2 GHz.

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**REFERENCES**